



## ANDpSi056ET0S

### 5.61" WSVGA Color p-Si TFT LCD Module

The ANDpSi056ET0S is 1024 x 600 Color TFT display that utilizes new poly-silicon (p-Si) technology to provide a brighter, thinner and lighter display with high-resolution. The p-Si TFT technology allows the row and column LCD drivers to be fabricated directly on the LCD glass. This eliminates the need for discrete TAB drivers and also reduces the thickness, weight and overall size of the display. The 5.6" WSVGA resolution expands applications in mini-notebook PC's.

#### Features

- High Luminance
- Single CCFL, Sidelight type
- Replaceable structure of lamp units
- Analog scaling board attachable to LCD backward
- Recommendable inverter attachable to LCD backward
- WSVGA (1024 x 600 pixels color display)
- Applications: display size for hand-held mobile devices

#### Mechanical Characteristics

Item	Specification	Unit
Outline Dimensions	141.8(W) x 84.4 (H) x 7.5max(D)	mm
Number of Pixels	1024(W) x 600(H)	pixels
Active Area	122.88 (W) x 72(H)	mm
Pixel Pitch	0.120(W) x 0.120(H)	mm
Weight (approx.)	85	gram
Backlight	Single CCFL, Sidelight type	-

#### Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V <sub>DD</sub>	-0.3	+4.0	V
Input Signal Voltage	V <sub>IN</sub>	-0.3	V <sub>DD</sub> + 0.3	V
Operating Ambient Temperature	T <sub>OP</sub>	0	50	°C
Operating Ambient Humidity	H <sub>OP</sub>	10	90	%(RH)
Storage Temperature	T <sub>STG</sub>	-20	+60	°C
Storage Humidity	H <sub>STG</sub>	10	90	%(RH)
Operating Temperature for Panel	-	0	+60	°C

#### Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage <sup>1)</sup> I <sub>FL</sub> =4.0mA(rms)	V <sub>DD</sub>	3.0	3.3	3.6	V
	V <sub>FL</sub>	-	500	-	V(rms)
FL Start Voltage (Ta = 0°C)	V <sub>SFL</sub>	(1000)	-	(1500)	V(rms)
Common Mode Input Voltage <sup>2)</sup>	V <sub>CM</sub>	0.5	1.2	1.75	V
Differential Input High Threshold	V <sub>TH</sub>	-	-	100	mV
Differential Input Low Threshold	V <sub>TL</sub>	-100	-	-	mV
Current Consumption	*1(I <sub>DD</sub> )	-	(200)	-	mA
	*2(I <sub>FL</sub> )	-	4.0	(5.0)	mA(rms)
Pwr Consumption I <sub>FL</sub> =4.0mA(rms)	P	-	2.66	-	W

\*1) The module should be always operated within these ranges. The "Typ." shows the recommendable value.

\*2) Recommended transmitter:

#### Optical Characteristics (Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Contrast Ratio (CR)	(100)	(250)	-	-
Response Time (t <sub>ON</sub> + t <sub>OFF</sub> )	-	-	50	ms
Luminance (L) I <sub>FL</sub> =4.0mA(rms)	90	120	-	cd/m <sup>2</sup>

Product specifications contained herein may be changed without prior notice.

It is therefore advisable to contact Purdy Electronics before proceeding with the design of equipment incorporating this product.

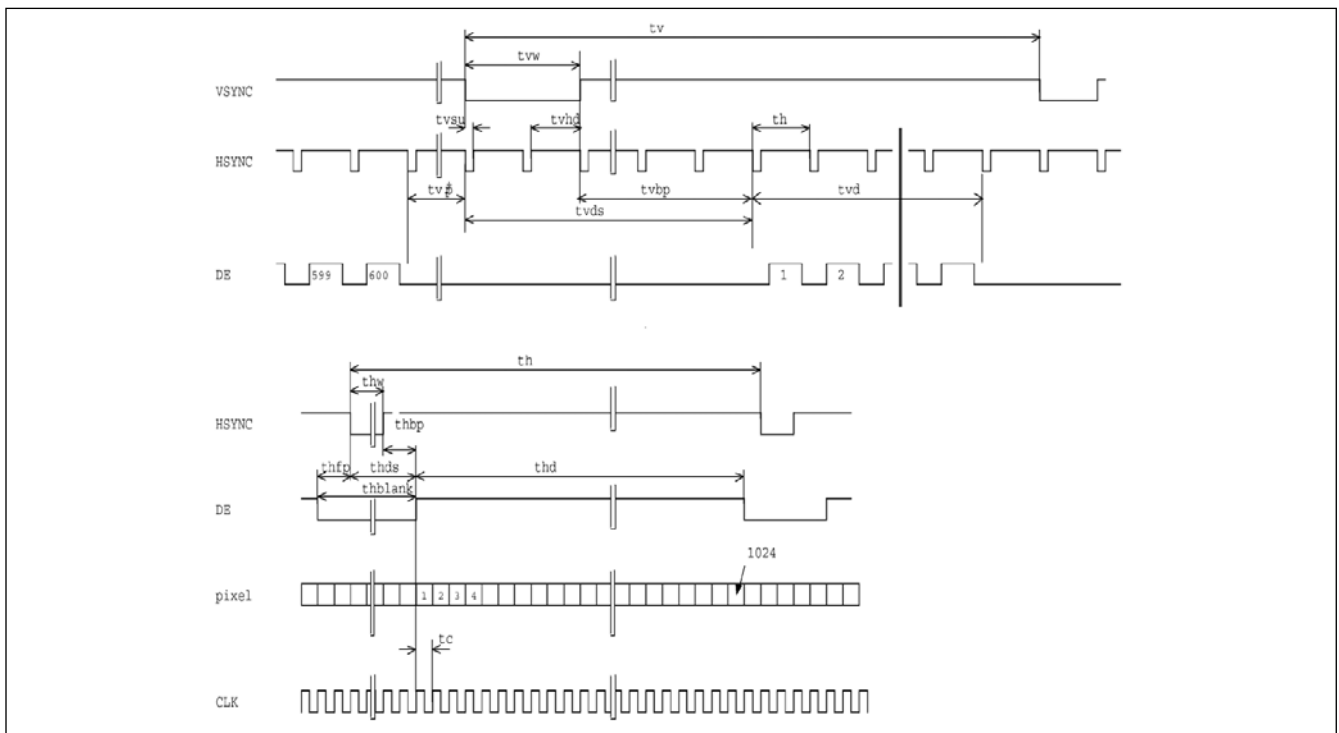


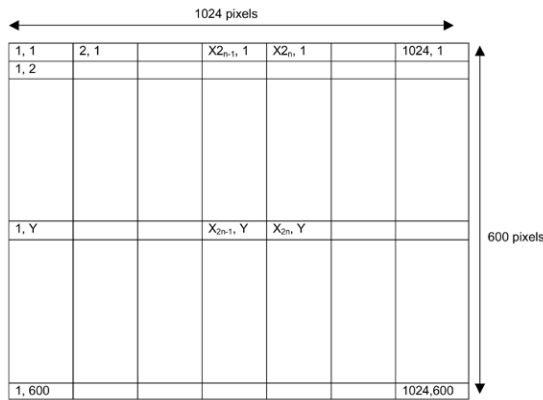
**Timing Specifications** (see Notes below)

Item	Symbol	Min	Typ	Max	Unit
Horizontal Scanning Term	$t_h$	$1334 \times t_c$	$1344 \times t_c$	–	clock
H-sync Pulse Width	$t_{hw}$	$8 \times t_c$	$136 \times t_c$	–	clock
Horizontal Front Porch	$t_{hfp}$	$4 \times t_c$	$24 \times t_c$	–	clock
Horizontal Back Porch	$t_{hbp}$	$24 \times t_c$	$160 \times t_c$	–	clock
Horizontal Data Sync Period	$t_{hds}$	$32 \times t_c$	$296 \times t_c$	–	clock
Horizontal Display Term	$t_{hd}$	$1024 \times t_c$	$1024 \times t_c$	$1024 \times t_c$	clock
Frame Period	$t_v$	$778 \times t_h$	$806 \times t_h$	$860 \times t_h$	line
V-sync Pulse Width	$t_{vw}$	$2 \times t_h$	$6 \times t_h$	–	line
V-sync Set up Time (to H-sync)	$t_{vsu}$	$8 \times t_c$	–	–	clock
V-sync Hold Time	$t_{vh}$	$8 \times t_c$	–	–	clock
Vertical Front Porch	$t_{vfp}$	$1 \times t_h$	$3 \times t_h$	–	line
Vertical Back Porch	$t_{vbp}$	$2 \times t_h$	$29 \times t_h$	–	line
Vertical Data Sync Period	$t_{vds}$	$8 \times t_h$	$35 \times t_h$	–	line
Vertical Display Time	$t_{vd}$	$600 \times t_h$	$600 \times t_h$	$600 \times t_h$	line
Clock Period	$t_c$	15.0	15.38	–	ns

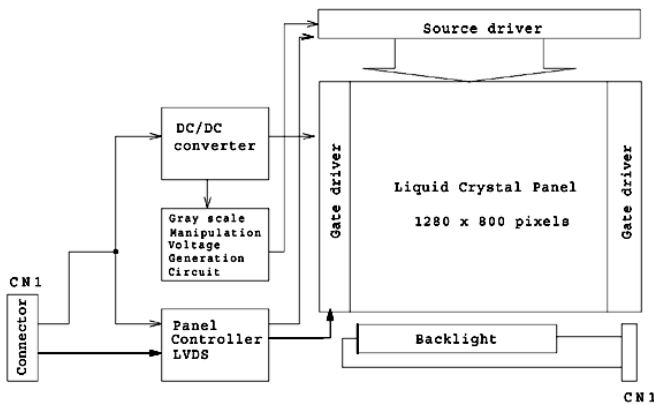
**Notes:**

Refer to "Timing Chart" below. If DE is fixed to "H" or "L" level for certain period while CLK is supplied, the panel displays black w/some flicker. If CLK is fixed to "H" or "L" level for certain period while DE is supplied, the panel may be damaged. Please adjust LCD operating signal timing and FL driving frequency, to optimize the display quality. There is a possibility that flicker is observed by the interference of LCD operating signal timing and FL driving condition (especially driving frequency), even if the condition satisfies above timing specifications and recommended operating conditions. Do not make  $t_v$ ,  $t_h$ ,  $t_{hbp}$  and  $t_{vds}$  fluctuate. If  $t_v$ ,  $t_h$ ,  $t_{hbp}$  and  $t_{vds}$  are fluctuate, the panel display black. In case of using the long frame period, the deterioration of display quality, noise, etc. may be occurred. CLK count of each Horizontal Scanning Time should be always the same. V-Blanking period should be 'n' X "Horizontal Scanning Time". (n:integer) Frame period should be always the same.

**Timing Chart**




**Block Diagram**



**Back View**



**Connector Pin Assignment for Interface**

CN1 Input Signal (see Notes below)  
 FH23-25S-0.3SHW(05) : gilding terminal /  
 Hirose Electric Co., Ltd.

Mating FPC : Use gilding terminal FPC

Terminal No.	Symbol	Function
1	V <sub>DD</sub>	Power Supply Voltage; 3.3V
2	V <sub>DD</sub>	Power Supply Voltage; 3.3V
3	V <sub>DD</sub>	Power Supply Voltage; 3.3V
4	V <sub>DD</sub>	Power Supply Voltage; 3.3V
5	GND	GND
6	GND	GND
7	GND	GND
8	GND	GND
9	RxCLK+	Pos. LVDS differential clock input
10	GND	GND
11	RxCLK-	Neg. LVDS differential clock input
12	GND	GND
13	RxIN2+	Pos. LVDS diff. data input, [B2-B5, V,H-sync, DE]
14	GND	GND
15	RxIN2-	Neg. LVDS diff. data input, [B2-B5, V,H-sync, DE]
16	GND	GND
17	RxIN1+	Pos. LVDS diff. data input, [G1-G5, B0-B1]
18	GND	GND
19	RxIN1-	Neg. LVDS diff. data input, [G1-G5, B0-B1]
20	GND	GND
21	RxIN0+	Pos. LVDS diff. data input, [R0-R5, G0]
22	GND	GND
23	RxIN0-	Neg. LVDS diff. data input, [R0-R5, G0]
24	GND	GND
25	GND	GND

**CN2 CCFL Power Source**

BHSR-02VS-1/Japan Solderless Terminal Mfg. Co., Ltd

Mating Connector : SM02B-BHS-1/Japan Solderless Terminal Mfg. Co., Ltd

Terminal No.	Symbol	Function
1	V <sub>FLH</sub>	CCFL Power Supply (High Voltage)
2	V <sub>FLL</sub>	CCFL Power Supply (Low Voltage)

Note (2): 256K colors are displayed by the combinations of 18 data bits.

	Display	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	Gray Scale Level
Basic Color	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	-
	Blue	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	-
	Green	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	-
	Lt. Blue	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	-
	Red	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	-
	Purple	H	H	H	H	H	H	L	L	L	L	L	L	H	H	H	H	H	H	-
	Yellow	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	-
White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	-	
Gray Scale of Red	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L1
		L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L2
	↕	:						:						:						L3~L60
		:						:						:						
	Light	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L61
		H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L62
Red	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	Red L63	
Gray Scale of Green	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L1
		L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L2
	↕	:						:						:						L3~L60
		:						:						:						
	Light	L	L	L	L	L	L	H	H	H	H	L	H	L	L	L	L	L	L	L61
		L	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	L62
Green	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	Green L63	
Gray Scale of Blue	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L1
		L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L2
	↕	:						:						:						L3~L60
		:						:						:						
	Light	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H	L61
		L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L	L62
Blue	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	Blue L63	
Gray Scale of White & Black	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	H	L1
		L	L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	H	L	L2
	↕	:						:						:						L3~L60
		:						:						:						
	Light	H	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	L	H	L61
		H	H	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	L	L62
White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	White L63	